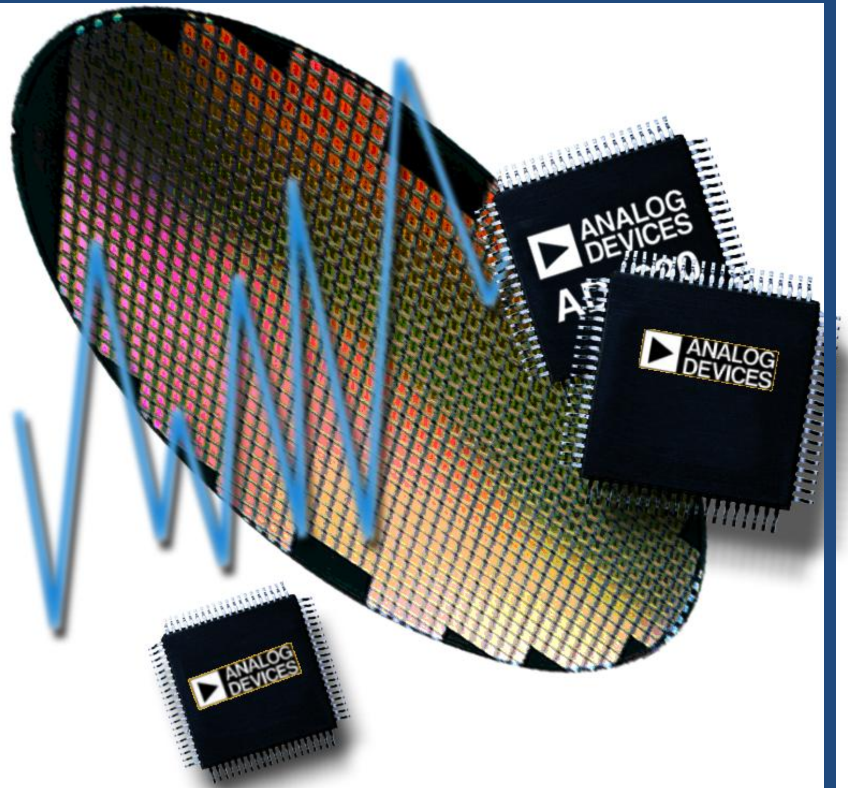

Reliability Report

Report Title: AD8607 at TSMC

Report Number: 8418

Revision: A

Date: 2 April 2010

Summary

This report documents the successful completion of the reliability qualification requirements for release of the AD8607 product in an 8-MINI_SO, and an 8-SOIC_N package. The AD8607 is a dual micro-power rail-to-rail input and output amplifier that features very low offset voltage as well as low input voltage and current noise.

Table 1: AD8607 Product Characteristics

Die/Fab

Die ID	6474
Die Size (mm)	1.39 x 1.83
Wafer Fabrication Site	TSMC Fab 9
Wafer Fabrication Process	0.6um CMOS
Transistor Count	Three thousand
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlSiCu
Die Overcoat	Polyimide

Package/Assembly

Available Package	8-MINI_SO	8-SOIC_N
Body Size (mm)	3.00 x 3.00 x 0.85	4.00 x 5.00 x 1.50
Assembly Location	Carsem-M	Amkor-P
Molding Compound	Sumitomo 6600H	Sumitomo 6600H
Wire Type	Gold Tanaka M3	Gold
Wire Diameter (mils)	1.00	1.00
Die Attach	Ablestik 84-1LMIS R4	Ablestik 84-1LMIS R4
Lead Frame Material	Copper	Copper
Lead Finish	Tin Plate	Tin Plate
Moisture Sensitivity Level	1	1
Maximum Peak Reflow Temperature (°C)	260	260

Description / Results of Tests Performed

Tables 2, 3 and 4 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 3: MINI_SO Package Qualification Test Results

Test Name	Spec	Conditions	Device	Lot #	Sample Size	Qty. Failures
Autoclave (AC)[1]	JESD22-A102	121°C 100%RH 2atm 96 hours	AD8275	Q7753.7	77	0
				Q7753.8	77	0
			AD8656	Q7055.1	77	0
				Q7055.5	77	0
				Q7055.6	77	0
			AD8692	Q7248.2	77	0
				Q7248.3	77	0
				Q7248.4	77	0
			ADA4505-2	Q7200.10	77	0
				Q7200.8	77	0
				Q7200.9	77	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	AD8656	Q6888.10	77	0
				Q6888.8	77	0
				Q6888.9	77	0
				Q7055.14	77	0
				Q7055.15	77	0
				Q7055.3	77	0
			AD8692	Q7248.10	77	0
				Q7248.8	77	0
				Q7248.9	77	0
			AD8617	Q7277.2	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C 1,000 hours	AD5660	AC49684.1	77	0
			AD8692	Q7248.12	77	0
				Q7248.13	77	0
				Q7248.14	77	0
			AD8656	Q7055.13	45	0
				Q6888.14	44	0
			ADA4505-2	Q7200.11	77	0
				Q7200.12	77	0
				Q7200.13	77	0
Solder Heat Resistance (SHR)[1]	ADI-0049	See Footer	AD8607	Q8418.104	30	0
				Q8418.105	30	0
				Q8418.106	30	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C 500 cycles	AD8652	Q7278.6	77	0
			AD8617	Q7277.6	77	0
			ADA4505-2	Q7200.6	77	0
			AD8132W	Q7332.13	77	0
				Q7332.14	77	0
			OP2177	AC80440.1	45	0
			AD5660	AC49678.1	77	0
			AD8692	Q7248.19	77	0
				Q7248.20	77	0
				Q7248.21	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125ºC
- Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Table 3: SOIC_N Package Qualification Test Results

Test Name	Spec	Conditions	Device	Lot #	Sample Size	Qty. Failures
Autoclave (AC)[1]	JESD22-A102	121°C 100%RH 2atm 96 hours	ADR02	Q6969.12	77	0
				Q6969.13	77	0
				Q6969.2	77	0
			AD8276	Q7770.2	77	0
			AD5824B	f161158.3	77	0
				f161176.3	77	0
				f161184.3	77	0
			AD8599	AB73284.1	77	0
			ADA4692-2	Q7559.1	77	0
				Q7559.2	77	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	ADA4627-1	Q7472.6	77	0
				Q7472.7	77	0
				Q7472.8	77	0
			AD8629	Q7100.14	77	0
				Q7100.15	77	0
				Q7100.16	77	0
			OP291	AC24671.1	77	0
				AC24687.1	77	0
				AC24688.1	77	0
				AC24689.1	77	0
			ADA4692-2	Q7559.4	77	0
				Q7559.5	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C 1,000 hours	ADA4627-1	Q7472.5	77	0
			AD8629	Q7892.3	45	0
			AD8210	Q6106.27	77	0
				Q6106.44	77	0
			AD8599	AC82781.1	77	0
			ADA4692-2	Q7559.6	77	0
			ADR02	Q6969.8	45	0
			OP291	AC24679.1	77	0
				AC24696.1	77	0
Solder Heat Resistance (SHR)[1]	ADI-0049	See Footer	AD8607	Q8418.104	30	0
				Q8418.105	30	0
				Q8418.106	30	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C 500 cycles	AD8629	Q7892.5	77	0
			AD8622	Q7323.18	77	0
			AD8276	Q7770.6	77	0
			AD8622	Q7323.18	77	0
			ADA4627-1	Q7472.12	77	0
				Q7472.13	77	0
				Q7472.14	77	0
			ADA4692-2	Q7559.7	77	0
				Q7559.8	77	0
			AD8656	Q7589.3	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125ºC
- Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Table 4: 0.60um CMOS Fab Qualification Test Results

Test Name	Spec	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, Method 1015	125°C Biased 48 hours	ADE7753	Q7670.0202	250	0
				Q7670.0203	250	0
				Q7670.0204	250	0
				Q7670.0205	250	0
				Q7670.0206	245	0
				Q7670.0207	250	0
				Q7670.0208	250	0
				Q7670.0201	250	0
			ADuM1402	Q8062.392	300	0
				Q8062.394	292	0
				Q8062.395	295	0
				Q8062.396	300	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	AD8630	Q7954.13	77	0
				Q7954.14	77	0
				Q7954.15	77	0
			AD8692	Q7248.8	77	0
				Q7248.9	77	0
				Q7248.10	77	0
			ADA4692-2	Q7559.13	77	0
				Q7559.4	77	0
				Q7559.5	77	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C ‹ Tj ‹ 135°C, Biased 1,000 hours	AD8601	Q7454.5	77	0
				Q7454.6	77	0
			AD7873	Q7321.9	77	0
				7321.8	77	0
		150°C ‹ Tj ‹ 175°C, Biased 500 hours	ADA4505-2	Q8001.1	77	0
				Q8001.6	77	0
			AD8601	Q7507.3	77	0
High Temperature Operating Life (HTOL)[1]	JESD22-A108	125°C ‹ Tj ‹ 135°C, Biased 1,000 hours	AD8648	Q7588.8	77	0
				Q7588.7	77	0
		150°C ‹ Tj ‹ 175°C, Biased 500 hours	AD8605	Q6728.5	77	0
			AD8692	Q7248.11	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125ºC
- Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field Induced Charge Device Model (FICDM) ESD testing are summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at the Analog Devices' web site).

Table 5: AD8607 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	8-MINI_SO	ANSI/ESD STM5.3.1-1999	1Ω, Cpkg	±1500V	NA	C6
	8-SOIC_N			±1500V	NA	C6
HBM	8-SOIC_N	ANSI/ESD STM5.1-2007	1.5kΩ, 100pF	±2000V	±2500V	2

Latch-Up Test Results

Six samples of the AD8607 were Latch-up tested at T_A=25°C per JEDEC Standard JESD78, Class I, Level A. All six devices passed.

Approvals

This report has been approved by electronic means (5.0).
Reliability Engineer: Robert Yhap

Additional Information

Data sheets and other additional information are available on Analog Devices' web site.